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Evaluating Protection Circuits and Test Methods

ESD

by Joe Salvador

Electrostatic discharge (ESD) protection is becoming an increasingly important issue to both semiconductor manufacturers and electronics equipment providers. Electronics equipment such as cellular phones, digital televisions and notebook computers are increasingly subjected to ESD events as users carry them around and constantly connect and disconnect them. Simultaneously, semiconductor manufacturers are finding it more difficult to provide even modest levels of on-chip ESD protection as silicon geometries shrink and advanced digital chips become more prone to ESD damage.

A growing need for ESD protection circuits is being seen across the industry, using a wide variety of technologies including diode arrays, varistors, and polymers. Unfortunately, a great deal of confusion exists as to what levels of ESD protection are appropriate, how systems should be designed and tested to ensure acceptable system reliability, and even on how to evaluate protection circuits. Eliminating some of this confusion is a necessary first step towards designing more reliable system.

ESD Paradox: Increasing ESD Events, Decreasing On-Chip Protection

Mobile electronics devices and interconnectivity are now commonplace. Cell phones, notebook computers and digital cameras are obviously subjected to many ESD events every day as they are handled by end users, but even non-mobile devices such as desktop PCs and LCD TVs are subjected to constant ESD stress as users plug cameras, games, and other devices into their USB and video ports. A simple act, such as walking across a synthetic carpet and touching an exposed port on the outside of a digital TV, can result in an ESD discharge greater than 35 kV.

ESD discharges can occur directly at the port, or they can be discharged through a cable. This scenario is particularly dangerous to the electronics equipment because the entire charge bypasses the connector’s ground shield (if it has one) and is discharged directly into the system’s electrical circuits.

At the same time, semiconductor devices are becoming increasingly sensitive to ESD. ESD damage can occur due to excessive voltage, high current levels, or a combination of both. High voltages can cause gate oxide punch-through, while excessive I²R levels can cause junction failures and metallization traces to melt. As manufacturing geometries decrease, the voltage and current levels that can cause these failures also decrease. This has made it difficult to provide even relatively low levels of on-chip ESD protection.

The increased susceptibility to ESD damage has been widely publicized recently, in part due to the efforts of the semiconductor industry itself. For example, the Industry Council on ESD Target Specifications, which includes 16 semiconductor companies, recently announced they were working on efforts to reduce the standard level of on-chip

ESD protection because it was hindering the industry’s ability to design and quickly bring to market high speed and high performance integrated circuits.

The focus of the Industry Council’s efforts is to reduce the level of on-chip ESD protection, primarily aimed at providing adequate levels of ESD protection for manufacturing environments. They are not suggesting reducing system level ESD protection, which they suggest must remain at existing levels.

Examples of Static Voltage Generation At Different Levels of Relative Humidity		
Means of Generation	10-25% RH	65-90% RH
Walking across carpet	35,000V	1,500V
Walking across vinyl tile	12,000V	250V
Worker at bench	6,000V	100V
Poly bag picked up from bench	20,000V	1,200V
Chair with urethane foam	18,000V	1,500V

Figure 1: Static Voltage Generation Examples (Source: ESD Association)

Relevant ESD Standards

Achieving adequate ESD protection in the face of increased ESD events and higher levels of semiconductor ESD vulnerability presents a challenge to the equipment manufacturer. However, before discussing approaches to providing ESD protection, it is important to first understand the relevant ESD standards and how they are meant to be used.

Semiconductor vendors often quote the levels of on-chip ESD protection they provide, using standards such as the Human Body Model (ESD STM5.1-1998) or the Machine Model (ESD STM5.2-1999). These standards are meant to indicate the levels of ESD that the chip can withstand in the manufacturing environment. Currently, most high

performance semiconductors are manufactured to meet a 2KV discharge per the Human Body Model. These standards are not adequate or even relevant to the levels of protection required at the system level. For system level ESD protection, the relevant standard is IEC 61000-4-2.

Unfortunately, these standards are often misunderstood and even used interchangeably, and are frequently misquoted in technical literature. A 2KV discharge per the Human Body Model is not the same as a 2KV discharge per the IEC 61000-4-2 standard, and a chip protected to 2KV HBM could easily be damaged at a 2KV IEC 61000-4-2 strike.

A key difference between these standards is the peak current level associated with a strike. As seen in Figure 2, the peak current discharged during an 8KV HBM strike is less than the peak current discharged during a 2KV IEC 61000-4-2 strike and, at 8KV (a common system level ESD requirement), the peak current for an IEC 61000-4-2 strike is over 22 times higher than what most high performance semiconductors are designed to withstand.

Another key difference between these standards is the rise time of the ESD pulse. An ESD pulse using the HBM model has a rise time of 25 nS, whereas the rise time of an IEC 61000-4-2 pulse is less than 1 nS (see Figure 3). This means that a protection circuit designed to withstand an HBM pulse

Applied Voltage (kV)	Peak Current (A) Human Body Model	Peak Current (A) IEC 61000-4-2
2	1.33	7.5
4	2.67	15.0
6	4.00	22.5
8	5.33	30.0
10	6.67	37.5

Figure 2: Peak current of HBM vs. IEC 61000-4-2 ESD standards



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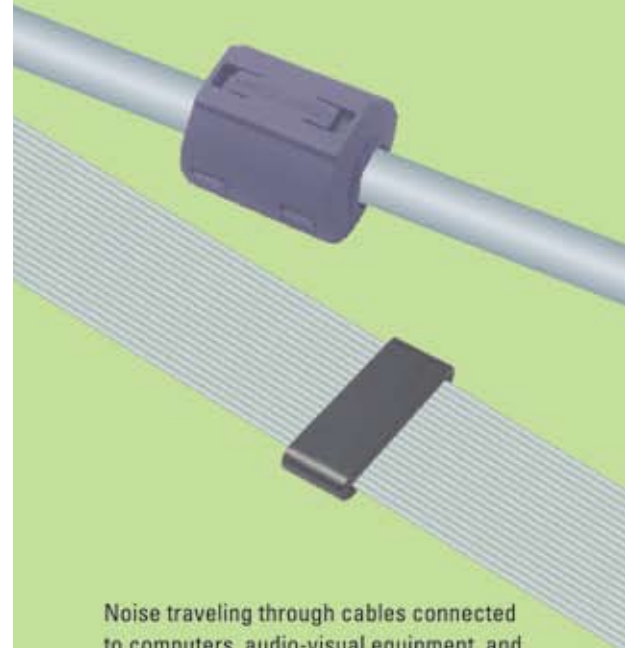


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may not even turn on before the “protected” chip is destroyed in an IEC 61000-4-2 pulse.

In short, most semiconductor devices are designed to withstand ESD events that may occur in a typical manufacturing environment. The ratings they use to characterize these chips, such as the Human Body Model or the Machine Model, have nothing to do with the levels of protection required in a system environment that is being shipped to the end user.

For system level ESD protection, the IEC 61000-4-2 model should be used, and almost all high performance semiconductor devices need some form of external ESD protection to prevent ESD damage coming in from exposed I/O ports.

ESD Protection Options

The system designer can use several techniques for providing ESD protection. To start, good mechanical design such as covers over I/O ports and recessed ports can reduce the number of ESD strikes that enter the system. In addition, many I/O connectors are designed so that there is an external ground shield on the connector and with pins that are recessed. Examples of well-designed connectors include USB and HDMI (a digital video interface).

Unfortunately, good connectors do not shield all ESD strikes. Not only can an ESD strike bypass the ground shield during an air discharge, it can also be injected directly into the port during a hot-plug event such as attaching a cable. The cable itself can be a source of discharge, as the cable may have built up a charge on it prior to being attached. Finally, the device on the other end of the cable may have a charge built up on it and, as it is attached, the ESD pulse can travel through the cable, bypassing the ground shield and damaging the semiconductor device itself.

Using the above HDMI connector as an example, imagine a scenario where an end user is trying to connect a new HDMI-based DVD recorder to an

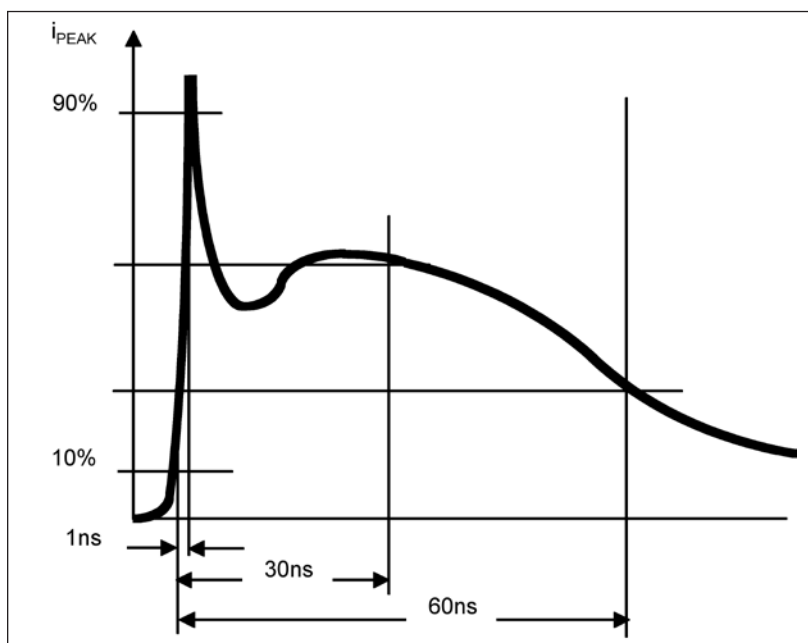


Figure 3: IEC 61000-4-2 ESD pulse waveform

older digital TV that uses a DVI connector. Electrically, these interfaces are the same, and DVI to HDMI adapters are commonly sold in most electronics stores. Yet, as can be seen

in Figure 4, the DVI connector has exposed pins that are easily accessible by and end user – in fact, it is a high probability that the end user will touch these pins while connecting it to another device, injecting an ESD event through the cable, bypassing the HDMI ground shield, and possibly damaging the new DVD player.



Figure 4: ESD probe easily contacts exposed pins of DVI connector

For these reasons, most manufacturers of consumer electronics, PCs, cellular phones, and other electronic equipment will typically use ESD protection circuits in their designs to complement the connector’s inherent protection and the on-chip protection of the high performance semiconductors, especially for ports such as USB and HDMI that are intended for “high touch” consumer applications.

ESD System Level Testing Methods

The IEC 61000-4-2 standard defines four standard levels of ESD protection, using two different testing methodologies. Contact discharge involves discharging an ESD pulse directly from the ESD test gun that is touching the device under test. This is the preferred method of testing. However, the standard provides for an alternate test methodology known as air discharge for cases where contact discharge testing is not possible. In the air discharge test, the ESD test gun is brought close to the device under test until a discharge occurs. The standards are defined so that each level is considered equivalent – a Level 4 contact discharge of 8KV is considered equivalent to a 15KV air discharge.

Historically, electronics equipment manufacturers have used the air discharge methodology for testing their systems on ports such as USB where the pins are recessed and difficult to access directly with an ESD discharge gun. However, this method has proven inadequate and is being replaced by many manufacturers with more reliable testing methodologies.

To understand why this practice is changing, it is helpful to visualize what happens during an air discharge test to see why it is so unreliable. Consider the system below, consisting of an I/O port connector, an application-specific integrated circuit (ASIC) with an I/O controller, and an ESD protection device. The purpose of testing



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this device is to determine whether the ESD protection device is sufficient to protect the ASIC from damage if an ESD strike enters the system.

Unfortunately, an air discharge test is unlikely to do this. As the ESD gun approaches the port, it is likely that the ESD discharge will strike the exposed ground shield rather than enter the system, since this is exactly what the ground shield on the connector is supposed to do. Figure 7 shows physically why this happens:

However, this says nothing about what happens to an ESD strike that gets past the ground shield or enters the system through the cable.

Many system vendors have found that they shipped systems they thought were protected based on air discharge testing methods, only to see damaged systems returned once they had been shipped to end users. For this reason, many system vendors are changing their ESD test methods to inject ESD strikes directly into the signal pins to bypass the external ground shield and to determine if the internal ESD protection circuits are sufficient. This can be done by several methods.

One method commonly used is to insert a cable into the connector, cut the cable and expose the individual wires connected to each signal. The ESD pulse can then be tested on each exposed wire, bypassing the ground shield and testing whether the system's ESD protection is adequate. This is now widely being adopted for testing USB port protection in the computing and consumer electronics industries.

Other methods include soldering an extension to the signal pin to allow a direct contact discharge to the signal pin or, in cases like HDMI, using an adapter such as DVI that allows direct contact to the signal pin.

In all cases, the purpose is to do a real-world test in the lab, prior to product shipping, to ensure that the port is adequately protected. As can be seen in Figure 8, by injecting the strike directly into the signal line, the ESD pulse bypasses the ground shield and enters the system. This test reveals whether the ESD protection device, coupled with the ASIC it is protecting, can provide adequate and reliable ESD protection once the system is shipped.

Choosing an ESD Protection Device

There are several types of ESD protection devices available today, but the most common can be divided into three categories: varistors, polymers, and diodes. The most difficult task in determining which ESD protection device to choose is one that should be the easiest – that is, figuring out which device will provide the greatest protection.

Ideally, this would be obvious in the datasheets from manufacturers of these devices, but unfortunately it often is

Contact Discharge		Air Discharge	
Level	Test Voltage kV	Level	Test Voltage kV
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
x ¹⁾	Special	x ¹⁾	Special

"x" is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.

Figure 5: IEC61000-4-2 test levels

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not. In addition, many system design engineers do not know which factors are important when choosing an ESD device.

Most ESD protection devices provide ESD level ratings in their datasheets. Often, system vendors compare these devices using these ratings. For example, device X may say 8KV, device Y says 15KV, so device Y is better – or is it? In reality, these ratings say almost nothing about how well the device will protect the system.

ESD ratings for protection devices say only what the device itself will survive, not what the system will survive. Obviously, the protection device must survive the ESD strike in order to provide ongoing protection. However, this is only one of several factors that need to be evaluated.

In addition to the ESD rating level of the protection device, the system vendor needs to consider what voltage level (clamping voltage) and how much current (residual current) will be seen by the ASIC. ESD protection devices function by shunting most (but not all) of the current to ground and “clamping” the voltage seen at the ASIC to a lower value than the strike voltage.

Determining the clamping voltage and residual current is not an easy task. The clamping voltage quoted in most ESD protection datasheets – if they are there at all – is often misleading. The residual current is never quoted, because it is a product of the system layout rather than of the device itself. As a proxy, using the protection circuit’s dynamic resistance

(R_{dyn}) can help compare devices, since a device with lower resistance will shunt a higher proportion of the current. Unfortunately, this value is usually not even mentioned in protection datasheets.

Comparing Clamping Voltages

The current industry practice is to publish clamping voltages based on a pulse with an 8uS rise time and a 20uS duration. Most datasheets will publish their clamping voltage using a 1A pulse and sometimes a higher current pulse as well. It is very important to note that this pulse has nothing to do with an ESD pulse, which has a 1nS rise time and a 60nS duration. In addition, the clamping voltage seen during a level 4 IEC 61000-4-2 strike with a peak current of 30 Amps has nothing to do with a 1A pulse.

However, since this is often the only data available when looking at datasheets, it is at least a good starting point for comparing different ESD protection devices.

In general, semiconductor diodes have the lowest peak clamping voltages, while varistors and polymers have clamping voltages significantly higher. Using the standard 1A pulse described above, most semiconductor ESD protection diodes are rated to clamp between 8 and 15 V. Based on our experience, when confronted with an 8KV IEC 61000-4-2 strike, these diodes will show peak clamping voltages of 50 to 100V, depending on other diode characteristics such as dynamic resistance.

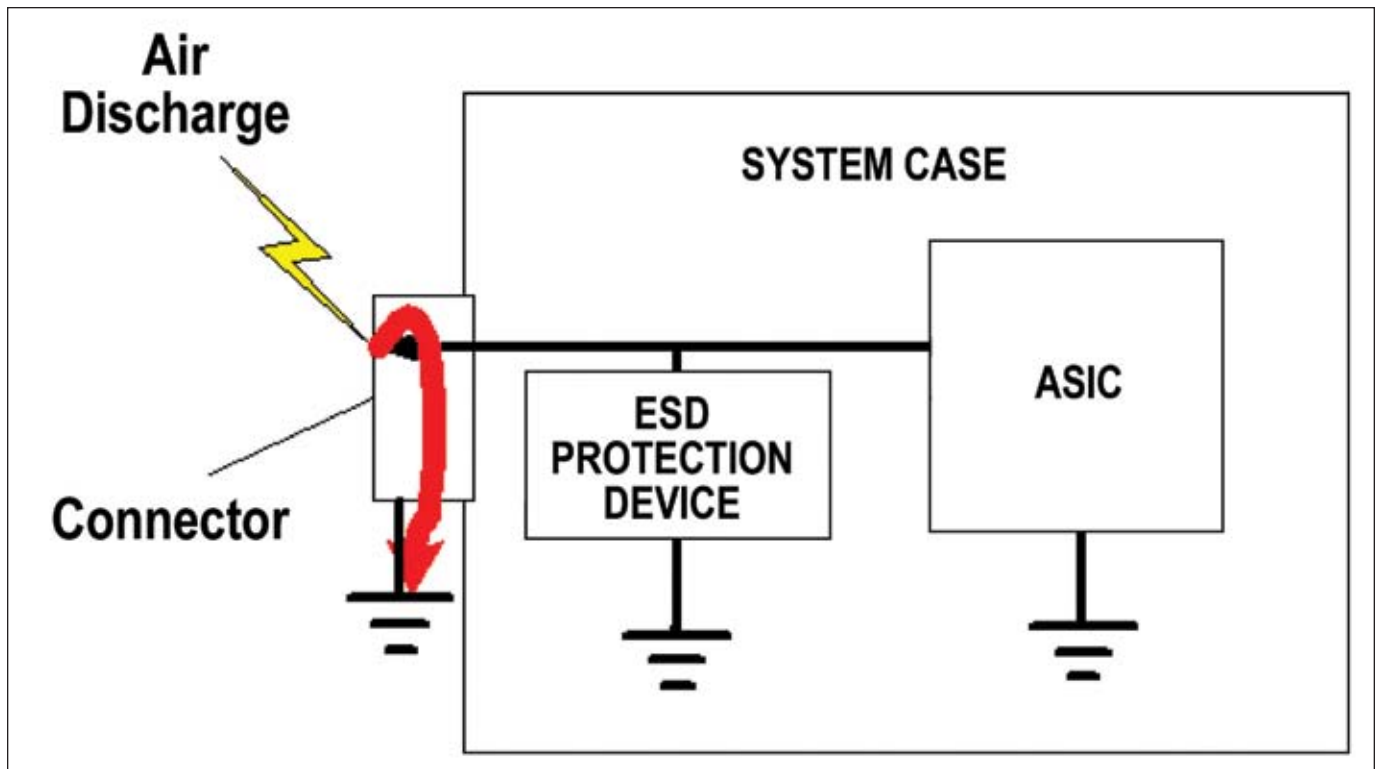


Figure 6: Air discharge fails to test ESD protection circuit



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In contrast, varistors can be several times higher – typical low capacitance varistors can have clamping voltages that range from 150 to 500V. Polymer devices suffer from even higher clamping voltages, due to a need for a “trigger” voltage. Common polymer protection devices can have a trigger

voltage as high as 500V. This need for a higher trigger voltage also inhibits the turn-on time of the polymer, increasing the likelihood of damage to the protected device.

In general, because of their lower clamping voltages and faster turn-on times, semiconductor diodes provide better ESD protection than either polymer or varistor solutions.

Residual Current and Dynamic Resistance

The amount of current flowing through to the ASIC is dependent on the dynamic resistance through the protection circuit vs. the dynamic resistance through the ASIC. As the resistance through the protection circuit increases, the amount of current flowing through the protected device increases proportionally, increasing the likelihood of damage.

Conversely, as the dynamic resistance of the ASIC decreases (such as might be the case if a low resistance ESD path exists on-chip within the ASIC), the residual current flowing through the ASIC will increase. This leads to the paradox that having a better on-chip ESD circuit can sometimes result in more damage than having no on-chip ESD circuits!

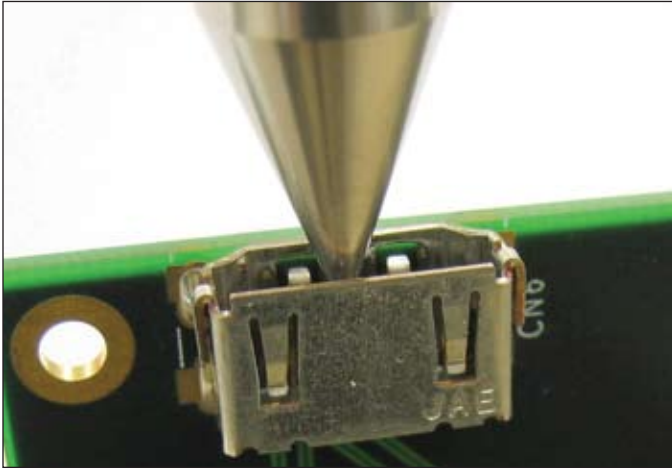


Figure 7: ESD probe hits ground shield rather than signal pins

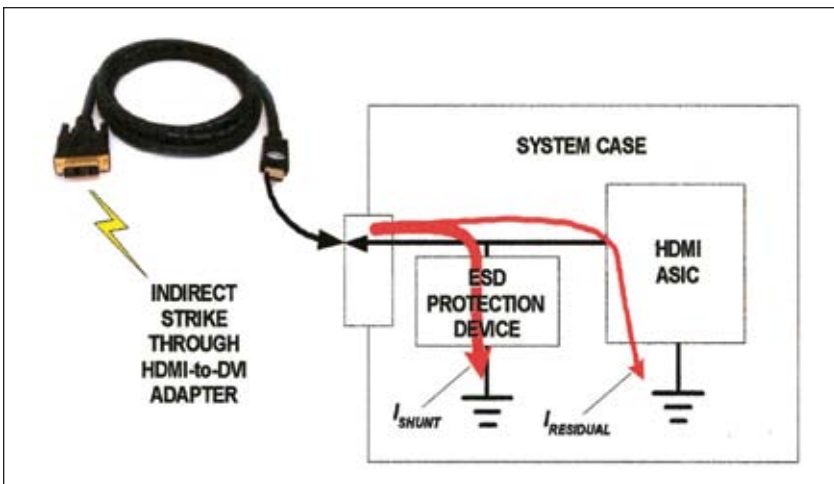


Figure 8: Real-world ESD system test

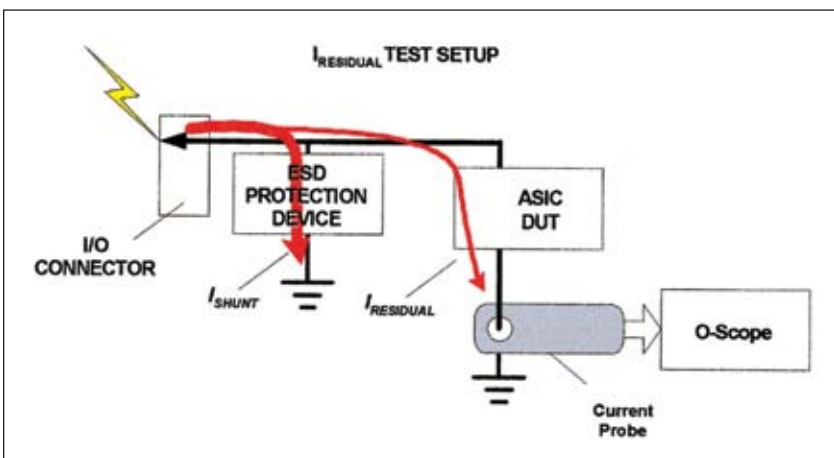


Figure 9: Test setup for measuring residual current seen at ASIC

In most cases, the system vendor is using a third party ASIC, so their key decision is to choose an ESD protection device that will shunt as much current as possible and minimize the residual current seen at the ASIC.

Because residual current is system dependent, it is not specified in any ESD protection datasheets. Unfortunately, very few ESD protection vendors specify their dynamic resistance either, but there are ways to approximate these values.

Many diode vendors will provide graphs of current vs. voltage. While these graphs are usually done using 8/20uS pulses rather than IEC 61000-4-2 pulses, they can be used as general indicators of the resistance of the circuit. For 8/20 uS pulses, the relationship between current and voltage is fairly linear, and the slope of the line is the dynamic resistance (R_{dyn}). Typical ESD diodes have R_{dyn} that can range from less than 1 ohm to 3 ohms. Polymer devices, once they turn on, also have very low resistance.

Varistors, in contrast, especially low capacitance varistors designed for high speed I/O ports, tend to have very high dynamic resistance. These can measure in the range of 20 ohms or more, resulting in much higher current levels seen at the protected ASIC.

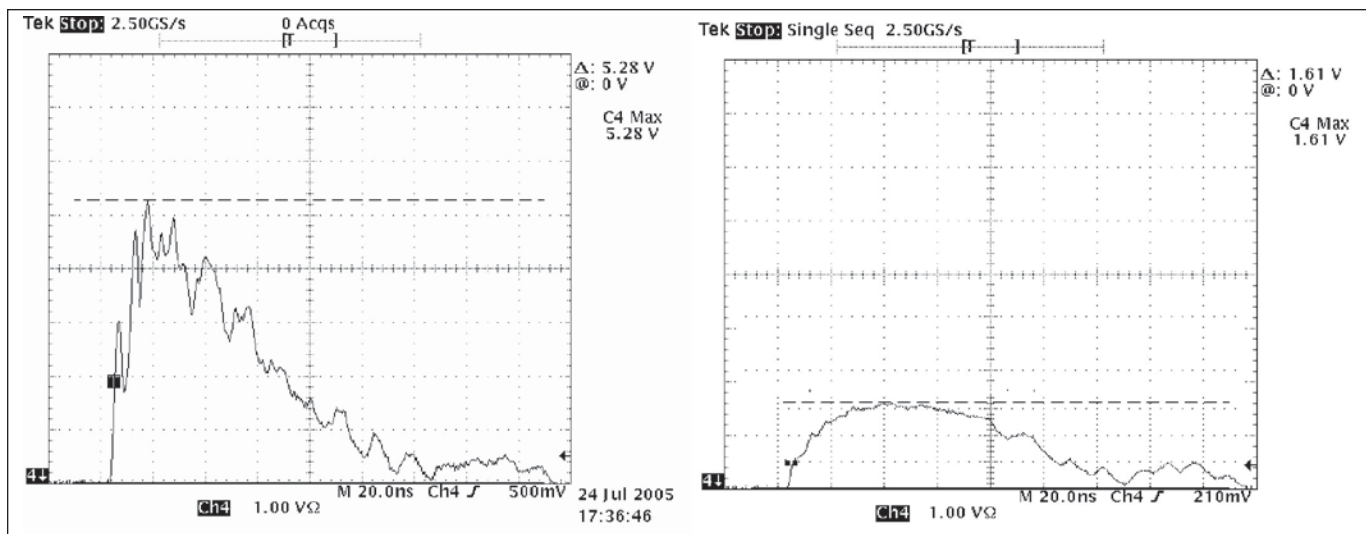


Figure 10: Residual current in varistor vs. diode circuit

Figure 10 shows the results from a system test comparing the levels of residual current seen at a specific HDMI ASIC when protected by a low capacitance varistor vs. a low capacitance diode. The test was done with a 4KV pulse and shows the current that flowed through the ASIC device.

In this case, the peak residual current was 10.6A when protected by varistors, vs. 3.2A when protected by semiconductor diodes. Also, just as importantly, the current seen at the ASIC during the entire duration of the strike was significantly higher in the varistor-based circuit. This illustrates the importance of comparing dynamic resistance when choosing ESD protection devices.

Next Steps

ESD protection is becoming increasingly critical as semiconductor geometries shrink and consumer usage of mobile electronics continues to increase. To help electronics system designers and manufacturers, the industry needs to formalize test methodologies which are already moving beyond the established standards of the last decade. Manufacturers of ESD protection devices also need to improve their specification methods to standardize key parameters such as clamping voltage and residual current. Finally, as semiconductor geometries continue to shrink and data rates continue to increase, new methods of ESD protection need to be developed to provide even greater protection without interfering with high speed signals. □

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